

IN THE CLAIMS

What is claimed is:

- 1 **1.** A memory cell, comprising:
 - 2 a first node for storing a first potential;
 - 3 a second node for storing a second potential; and
 - 4 a capacitor having plates coupled between the first node and
 - 5 second node, a portion of at least one plate of the capacitor comprising a
 - 6 first interconnect wiring that interconnects circuit components of the
 - 7 memory cell.

- 1 **2.** The memory cell of claim 1, further comprising:
 - 2 a first inverter having an input coupled to the first node and an
 - 3 output coupled to the second node; and
 - 4 a second inverter having an input coupled to the second node
 - 5 and an output coupled to the first node; wherein
 - 6 the first node stores a true data value and the second node
 - 7 stores a complementary data value.

- 1 **3.** The memory cell of claim 1, further including:
 - 2 a first access transistor coupled to the first node; and
 - 3 a second access transistor coupled to the second node.

1 **4.** The memory cell of claim 1, further including:
2 transistor gates formed from a gate layer; and
3 the first conductive interconnect wiring is formed over the gate layer
4 and includes a plurality of conductive layers, at least one of the conductive
5 layers forming at least a portion of a first plate of the capacitor.

1 **5.** The memory cell of claim 4, wherein:
2 the first conductive interconnect wiring includes a bottom
3 conductive layer, a dielectric layer formed over the bottom conductive
4 layer, and a top conductive layer formed over the dielectric layer, the top
5 conductive layer forming at least a portion of the first plate of the
6 capacitor.

1 **6.** The memory cell of claim 4, further including:
2 a second conductive interconnect wiring formed over the first
3 conductive interconnect wiring that forms at least a portion of a second
4 plate of the capacitor.

1 **7.** The memory cell of claim 6, wherein:
2 the second conductive interconnect wiring comprises titanium;
3 the bottom conductive layer comprises titanium nitride; and
4 the top conductive layer comprises titanium.
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1 **8.** A method of forming a capacitor in an integrated circuit, comprising the steps of:
2 depositing an insulating layer over a plurality of capacitor
3 structures, each capacitor structure comprising a dielectric layer disposed
4 between a first interconnect layer and a second interconnect layer;
5 forming a recess in the insulating layer according to a capacitor
6 mask pattern to expose the second interconnect layer of at least two
7 capacitor structures; and
8 forming a third interconnect layer within the recess that is in
9 electrical contact with the exposed second interconnect layers of the at
10 least two capacitor structures.

1 **9.** The method of claim 7, wherein:
2 the insulating layer comprises silicon oxide.

1 **10.** The method of claim 7, wherein:
2 the third interconnect layer comprises titanium.

1 **11.** The method of claim 8, further including:
2 prior to depositing the insulating layer
3 forming the first interconnect layer;
4 forming the dielectric layer over the first interconnect layer;
5 forming the second interconnect layer over the dielectric layer;
6 and

7 etching through the first interconnect layer, the dielectric layer,
8 and the second interconnect layer to form the capacitor structures.

1 **12.** The method of claim 11, wherein:

2 the first interconnect layer comprises titanium nitride; and
3 the second interconnect layer comprises titanium.

1 **13.** The method of claim 11, wherein:

2 after forming the capacitor structures
3 depositing a spacer insulating layer over the capacitor
4 structures; and
5 anisotropically etching the spacer insulating layer to form
6 insulating spacers on side surfaces of the capacitor structures while
7 exposing the second interconnect layer of the capacitor structures.

1 **14.** The method of claim 8, further including:

2 the step of forming a recess in the insulating layer includes etching
3 a portion of the first insulating layer; and
4 after forming the third interconnect layer, chemical-mechanical
5 polishing to remove portions of the third interconnect layer outside of the
6 recess.

1 **15.** A method of forming an integrated circuit memory cell, comprising the steps of:

2 forming a first interconnect wiring that electrically connects a
3 plurality of transistor gates to transistor diffusion regions, the first
4 interconnect wiring pattern comprising at least one dielectric layer
5 between top and bottom conductive layers; and
6 forming a second interconnect layer over the first interconnect
7 wiring in electrical contact with the top conductive layers to form a
8 capacitor, the capacitor including a first plate comprising the top
9 conductive layer, a second plate comprising the second interconnect
10 layer, and a capacitor dielectric comprising the at least one dielectric layer.

1 **16.** The method of claim 15, wherein:

2 the step of forming the first interconnect wiring includes
3 forming the bottom conductive layer having a thickness of no more
4 than about 1000 angstroms;
5 forming the at least one dielectric layer having a total thickness of
6 less than about 80 angstroms;
7 forming the top conductive layer having a thickness of no more than
8 about 300 angstroms; and
9 etching through the bottom conductive layer, at least one dielectric
10 layer and the top conductive layer according to a first wiring pattern.

1 **17.** The method of claim 15, further including:

2 forming insulating sidewalls on the sides of the first interconnect

3 wiring.

1 **18.** The method of claim 17, wherein:

2 the step of forming insulating sidewalls includes

3 depositing a layer of silicon nitride having a thickness of no more

4 than about 500 angstroms; and

5 anisotropically etching the layer of silicon nitride.

1 **19.** The method of claim 15, wherein:

2 the first interconnect wiring includes

3 a first wiring portion that electrically connects a gate of at least a

4 first memory cell transistor to a source/drain region of a second memory
5 cell transistor, and

6 a second wiring portion that electrically connects a gate of at least a

7 second memory cell transistor to a source/drain region of the first memory
8 cell transistor.

1 **20.** The method of claim 19, wherein:

2 the first and second wiring portions are formed on an interconnect
3 insulator layer;

4 the first wiring portion is electrically connected to the gate of the
5 first memory cell transistor by a first local contact that extends through the
6 interconnect insulator layer; and

7 the second wiring portion is electrically connected to the gate of the
8 second memory cell transistor by a second local contact that extends
9 through the interconnect insulator layer.

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